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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Geun-Woo PARK

Serial No.:	08/922,300	Examiner:	M. Marc-Coleman
Filed:	2 September 1997	Art Unit:	2774

For: DISPLAY DEVICE WITH POWER INTERRUPTION DELAY FUNCTION

Appeal No. 2002-0587

The Honorable Commissioner
of Patents & Trademarks
Washington, D.C. 20231

ATTENTION: Board of Patent Appeals and Interferences

APPELLANT'S REQUEST FOR REHEARING (37 CFR §1.197(b))

Pursuant to 37 CFR §1.197(b), Appellant respectfully requests a rehearing of the above captioned appeal from the Decision on Appeal (Paper No. 25), mailed 28 February 2003.

This request is transmitted in triplicate (37 CFR §1.192(a)).

REPLY BRIEF

I. STATEMENT OF REAL PARTY IN INTEREST

Pursuant to 37 CFR §1.192(c)(1) the real party in interest is:

SamSung Electronics Co., Ltd.
416 Maetan-dong, Paldal-ku,
Suwon City, Kyungki-do,
Republic of Korea

II. RELATED APPEALS AND INTERFERENCES

Pursuant to 37 CFR §1.192(c)(2), there are no appeals nor interferences known to the Appellant, the Appellant's legal representative, or the Assignee (real party of interest) which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

The Examiner errs in stating that the Appeal Brief does not contain the foregoing statement.

III. STATUS OF CLAIMS

Claims 1-11 have been finally rejected and are appealed herein.

IV. STATUS OF AMENDMENTS AFTER FINAL REJECTION

No amendment has been filed after receipt of the final rejection (Paper No. 17).

V. SUMMARY OF THE INVENTION

Page 10, line 5 - Page 13, line 11

Fig. 3 is a detailed circuit diagram illustrating the construction of a display device with a

power interruption delay function in accordance with the present invention. In the display device of Fig. 3, the voltage source V1 is connected to the input terminal of the H/V processor constant voltage circuit 131 through the power interruption delay charging circuit 370.

The power interruption delay charging circuit 370 includes a reverse voltage prevention diode D1 having its anode connected to the voltage source V1 and its cathode connected to the input terminal of the H/V processor constant voltage circuit 131, and a polarity capacitor C1 having its positive pole connected to a connection point of the cathode of the reverse voltage prevention diode D1 and the input terminal of the H/V processor constant voltage circuit 131 and its negative pole connected to the ground voltage terminal.

The operation of the display device with the above-mentioned construction in accordance with the present invention will hereinafter be described in detail.

When the display device is powered on, the high voltage from the high voltage source B+ is charged on the horizontal deflection coil H-DY and S-correction capacitor Cs through the field effect transistor FET1 and pulse transformer PT in the current amplifier 136 and then discharged through the discharge loop including the horizontal output transistor TR in the horizontal output circuit 134. Such charging and discharging operations are repeated as stated previously with reference to Fig. 2.

If the power supply to the display device is interrupted during the operation of the display device, the voltage supply to the H/V processor constant voltage circuit 131 is at once stopped in the display device of Fig. 2, as shown in Fig. 4a. However, according to the present invention, a voltage, charged on the polarity capacitor C1 during the power supply, is applied to the input terminal of the H/V processor constant voltage circuit 131, as shown in Fig. 4b, while it is discharged. As a result, the H/V processor constant voltage circuit 131 does not immediately stop

the voltage supply to the H/V processor 132.

Noticeably, the reverse voltage prevention diode D1 is connected in series between the voltage source V1 and the H/V processor constant voltage circuit 131 to protect the power supply circuit by allowing the voltage charged on the polarity capacitor C1 not to be discharged to the voltage source V1 at the power interruption state.

Because the voltage charged on the polarity capacitor C1 is continuously applied to the H/V processor constant voltage circuit 131 until it is completely discharged, the voltage supply to the H/V processor 132 is not interrupted immediately. Therefore, the H/V processor 132 outputs the horizontal pulse signal continuously for a predetermined time period, as shown in Fig. 5b.

The continuous pulse output time of the H/V processor 132 is determined according to a discharge time of the polarity capacitor C1. As a result, the continuous pulse output time of the H/V processor 132 can be varied by adjusting the discharge time of the polarity capacitor C1.

While the output pulse from the H/V processor 132 maintains such a high voltage level as to continuously drive the field effect transistor FET2 in the horizontal driver 133, the horizontal drive transformer T2 continues to be excited to induce a voltage in its secondary coil, thereby causing the horizontal output transistor TR in the horizontal output circuit 134 to remain at its driven state. Hence, the high voltage charged on the horizontal deflection coil H-DY and S-correction capacitor Cs can be sufficiently discharged. Namely, the discharge time of the high voltage charged on the horizontal deflection coil H-DY and S-correction capacitor Cs is sufficient.

As apparent from the above description, according to the present invention, the power interruption delay charging circuit is provided at the input terminal of the H/V processor constant voltage circuit in the display device. The power interruption delay charging circuit can prevent the horizontal output transistor from being damaged due to an instantaneous surge current when power

supply is resumed after power interruption. Further, the power interruption delay charging circuit can prevent the peripheral devices and circuits from being successively damaged due to damage in the horizontal output transistor.

VI. ISSUES

Whether claims 1-11 are patentable under 35 U.S.C. §103(a) over Applicant's admitted prior art (*hereafter*: AAPA) in view of Van Clifton Martin '348 (*hereafter:* Martin).

A. In accordance with 37 CFR §1.197(b) the original decision of the Board of Patent Appeals and Interferences appears to have misapprehended or overlooked the following points and grounds for reversal of the final rejection in rendering its original decision.

1. The original decision of the Board errs with respect to the affirmation of the rejection of claim 1, and subsequently claims 2-1, due to an improper affirmation of the final rejection based on new grounds not presented in the final rejection (Paper No. 17) nor the Examiner's Answer (Paper No. 20). See 37 CFR 1.196(b).

B. In accordance with 37 CFR §1.197(b) the original decision of the Board of Patent Appeals and Interferences appears to have misapprehended or overlooked the following points and grounds for reversal of the final rejection in rendering its original decision.

1. It was error, as a matter of law, to cite Appellant's identification of the problems in prior art devices as the motivation to modify those devices to render the claimed invention obvious.
2. The original decision of the Board errs with respect to the affirmation of the rejection

of claim 1, and subsequently claims 2-11, due to an improper finding that Martin teaches modifying the AAPA to provide a power interruption delay charging means for gradually lowering an input voltage to a H/V processor constant voltage circuit when power supplied to a display device is interrupted.

VII. GROUPING OF CLAIMS

Claim 1 stands or falls alone, and claims 2-11 stand or fall with claim 1.

VIII. ARGUMENT

Claims 1-11 are not obvious and unpatentable under 35 U.S.C. §103(a) in view of the combined teachings of the AAPA and Martin.

A.1. The original decision of the Board errs with respect to the affirmation of the rejection of claim 1, and subsequently claims 2-1, due to an improper affirmation of the final rejection based on new grounds not presented in the final rejection nor the Examiner's Answer.

Martin's invention relates to a protection system for the screen of a cathode ray tube. Martin includes three protection control circuits 34, 35 and 36. In the final rejection and the Examiner's Answer the rejection did not apply any of the teachings in Martin regarding protection control circuits 34, 35 and 36, nor any of the teachings regarding how control circuit 36 relates to NPN transistor 56 and horizontal deflection yoke 17. Instead, the final rejection and the Examiner's Answer refer us to Martin's col. 2, lines 64-72, which state:

The control grid 14 is clamped to a negative DC bias voltage -V1 from the

> power supply by a diode 44 connected between voltage -V1 and the control grid 14 and a capacitor 45 connected between the control grid 14 and ground. The output of the unblank driver 22 thereby controls the voltage between the control grid 14 and the cathode 13 by controlling the voltage of cathode 13. This diode-capacitor network makes the voltage at the control grid 14 drop slowly even though its bias voltage -V1 is removed.

Note here, however, that Martin **does not** teach that diode 44 and cathode 45 function to **protect** the screen.

In affirming the rejection, the Board has applied Martin's teaching regarding protection control circuit 36 as it relates to NPN transistor 56 and horizontal deflection yoke 17. See page 8, line 1+.

There is no indication in the decision that the Board's affirmation was based solely on the grounds provided in the final rejection and Examiner's Answer. In fact it appears that the Board agreed with the Appellant that the Examiner's rationale failed to support the rejection. See page 7, line 27-page 8, line 1.

Therefore, although the reference on which the rejection is based remains the same, the basis for affirming the rejection is not founded on the same grounds set forth in the final rejection and the Examiner's Answer. As set forth in §1.196(b), "any grounds not involved in the appeal for rejecting any claim . . . constitutes a new ground of rejection of the claim."

Accordingly the affirmation of the final rejection is improperly based on new grounds not presented in the final rejection (Paper No. 17) nor the Examiner's Answer (Paper No. 20).

B.1. The rejection, as based on the Appellant's assessment of the prior art, is reversible error. A rejection under 35 USC §103 must be based on what was known prior to when the invention was made. The Appellant's assessment of the prior art, the problem confronted by the

inventor, was not known to any one prior to when the invention was made since there is no teaching of such an assessment except as set forth in the instant specification, and the instant specification was not known prior to when the invention was made.

There is no teaching in the prior art that it was known to one of ordinary skill in the art that the horizontal output circuit 134 in the AAPA or transistor TR in horizontal output circuit 134 in the AAPA was subject to damage when power supplied to a display device is interrupted. The only teaching is that provided by the Applicant's assessment wherein the specification states:

> As the H/V processor operates no longer, it outputs no pulse signal thereby causing the high voltage charged on the horizontal deflection coil and S-correction capacitor not to be discharged. As a result, a voltage of about +120 to 160 V remains.
>
> Under the above condition, if the power supply to the display device is resumed, the H/V processor constant voltage circuit is driven because of application of a voltage so as to operate the H/V processor, a high voltage with a very high peak value (about +1.5 to 1.8KV) is instantaneously generated. As a result, a surge current resulting from the instantaneous high voltage abruptly flows through a discharge loop damaging a portion of the horizontal output circuit.
>
> **If** the horizontal output circuit is damaged, no horizontal deflection is performed on the screen of the display device, thereby causing a single line to be vertically drawn on the center of the screen. As a result, the user cannot recognize the information displayed on the screen.
>
> Further, the peripheral devices and circuits may successively be damaged due to a short-circuit resulting from the damage in the horizontal output circuit. (Emphasis added)

The Board refers us, in particular, to Applicant's statement "**If** the horizontal output circuit is damaged, no horizontal deflection is performed on the screen of the display device, thereby causing a single line to be vertically drawn on the center of the screen. As a result, the user cannot recognize the information displayed on the screen." (Emphasis added) The term "If" fairly suggests that only the Applicant considers that a problem may occur do to the high voltage charged on the

horizontal deflection coil and S-correction capacitor not to being discharged.

An inventor's identification of a problem in the prior art can not be used as a evidence of motivation to modify the prior art. *In re Nomiya*, 184 U.S.P.Q. 607, at 612-13 (C.C.P.A. 1975). *In re Kaslow,* 707 F.2d 1366, 1373, 217 USPQ 1089, 1094-95 (Fed. Cir. 1983) (quoting *In re Sponnoble*, 405 F.2d 578, 585, 160 USPQ 237, 243 (CCPA 1969)).

B.2. The original decision of the Board errs with respect to the affirmation of the rejection of claim 1, and subsequently claims 2-11, due to an improper finding that Martin's teaching regarding protection control circuit 36 as it relates to NPN transistor 56 and horizontal deflection yoke 17 provides a *prima facie* basis of obviousness for modifying the AAPA.

Regarding claim 1, AAPA teaches all that is claimed except the feature of*power interruption delay charging means for gradually lowering said input voltage to said H/V processor constant voltage circuit when power supplied to said display device is interrupted,* which is deemed to be non-obvious in view of the proposed combination of art.

The present invention provides a power interruption delay charging means for gradually lowering an input voltage to the H/V processor constant voltage circuit when power supplied to a display device is interrupted in order to protect horizontal output circuit 134 consisting of transistor TR.

Assuming, *arguendo*, that it was known to one of ordinary skill in the art that then we must consider what Martin fairly teaches to one of ordinary skill in the art absent the teachings of the present application.

Martin notes a problem that a power loss could result in a **high beam current** and local

overheating of the screen, called phosphor or screen burn spots. See col. 1, lines 15-20. Martin provides three parallel protection circuits (34, 35 and 36) to prevent screen burn spots: 1) protection circuit 34 is a cathode control circuit that will inhibit the beam current by controlling the voltage produced by unblank driver 22 for cathode 13; 2) protection circuit 35 is an accelerator grid control circuit that functions to short any voltage at accelerator grid 15 to ground; and 3) protection circuit 36 is a horizontal deflection control circuit that horizontally deflects the beam off the screen while the voltage at accelerator grid 15 is decaying to zero.

1) Cathode control circuit 34 includes an AND gate 42 that prevents beam generation when protection is required. Martin **does not** teach that diode 44 and cathode 45 function to **protect** the screen or any other protection function.

2) Accelerator grid control circuit 35 is necessary to short accelerator grid 15 to ground because the capacitance in capacitor 46 would normally prevent an immediate drop to zero.

3) Horizontal deflection control circuit 36 includes a transistor 58, resistors 61 and 62, relay coil 65, and relay contact 64. To prevent screen burn spots, transistor 58 is turned on by the two bias voltages provided via resistors 61 or 62. These two bias voltages are arranged so that if one fails the other will be present. Also, the value of these bias voltages are chosen so that even if there is a power failure, the voltages decay off at a slow enough rate so that transistor 58 will be turned on long enough to cause the beam to be horizontally deflected off the screen, thereby preventing the beam from burning the screen.

In the Board's new ground of rejection, we are referred to Martin's discussion of horizontal deflection yoke 17 and protection circuit 36, *i.e.*, horizontal deflection control circuit 36. In normal operation deflection of the beam by yoke 17 is controlled by X-yoke drive 101 over line 55 at the

base of NPN transistor 56 which is connected between one side of the horizontal deflection yoke 17 and has a resistor 57 to ground..

Martin suggests that in order to avoid damage to the screen it is desired to cause the beam to be horizontally deflected off the screen. This is accomplished by protection circuit 36. In particular, a second NPN transistor 58 is normally off and is connected across transistor 56 with a current limiting resistor 59 connected therebetween. A positive DC bias voltage from the power supply +V3 is applied to the yoke 17. Transistor 58 is normally off and therefore current through transistor 56 controls the current through the horizontal deflection yoke 17 and thus the horizontal deflection of the beam. When it is necessary to protect the screen 16, the transistor 58 is turned on and additional current is drawn through the coil of the horizontal deflection yoke 17 so as to drive the beam off the screen.

According to the foregoing teaching found in Martin, one of ordinary skill in the art would have modified the AAPA to include a circuit similar to protection circuit 36 **in order to protect the screen** if it is shown that a similar problem would exist regarding the screen in the AAPA Here again, it appears that the Board relies on the Applicant's statement "If the horizontal output circuit is damaged, no horizontal deflection is performed on the screen of the display device, thereby causing a single line to be vertically drawn on the center of the screen."

There has been no factual showing that "causing a single line to be vertically drawn on the center of the screen" would damage the screen. Any holding that the screen in the AAPA would be damaged by the vertically drawn on the center of the screen results from speculation, not fact. Deficiencies in the factual basis cannot be supplied by resorting to speculation or unsupported generalities. *In re Warner*, 379 F.2d 1011, 154 USPQ 173 (CCPA 1967) and *In re Freed*, 425 F.2d 785, 165 USPQ 570 (CCPA 1970).

Accordingly, there is no *prima facie* showing of a need to modify the AAPA in view of Martin's teaching.

Assuming, *arguendo*, that "causing a single line to be vertically drawn on the center of the screen" would damage the screen. Modifying the AAPA to prevent such a line is taught by Martin, that teaching being to to drive the beam off the screen. Accordingly, one of skill in the art would further look to Martin's protection circuit 36 which has the function of to driving the beam off the screen.

Looking to the Board's decision, the paragraph spanning pages 12 and 13 refer to Martin's teaching regarding "the situation where the power supply fails" and that "Martin teaches that when the power supply fails, the horizontal deflection control circuit 36 provides protection by causing the voltage to transistor 58 to decay off at a slow enough rate to so that transistor 58 will be turned on to cause the beam to be horizontally deflected off the screen."

Therefore, any modification of the AAPA would entail connecting protection circuit (36 which includes transistor 58) to the AAPA's transistor TR of horizontal output circuit 134 in the same manner as taught by Martin. Thus any voltage charged on the horizontal deflection coil H-DY and S-correction capacitor Cs will be discharged.

Claim 1 requires that the power interruption delay charging means be provide for gradually lowering an input voltage to the horizontal/vertical processor constant voltage circuit 131 of the AAPA when power supplied to the display device is interrupted.

Martin's teaching fails to suggest such a modification of the AAPA, and the Board has failed to provide a *prima facie* basis of support for suggesting that such a modification would have been obvious.

Thus far, it has been shown that taking into account only what is taught by the prior art, there is no teaching which would have fairly suggested to one of ordinary skill in the art any reason to provide power interruption delay charging means for gradually lowering an input voltage to the horizontal/vertical processor constant voltage circuit 131 of the AAPA when power supplied to the display device is interrupted.

Looking to the Board's decision further, we have attempted to ascertain why the Board has suggested that providing power interruption delay charging means for gradually lowering an input voltage to the horizontal/vertical processor constant voltage circuit 131 of the AAPA when power supplied to the display device is interrupted would have been obvious.

It appears that the Board's statement on page 9, lines 13-17, *i.e.*, "we find Martin's additional teaching of slowly decaying the voltage to the horizontal deflection yoke would have suggested to an artisan gradually dropping the voltage of the voltage source V1 of the horizontal/vertical constant voltage circuit [131] of the [AAPA]" to be key to the Board's finding.

Looking again to Martin, we find no such teaching of "slowly decaying the voltage to the horizontal deflection yoke." Martin teaches slowly decaying the voltage to the control grid 14. Martin also teaches that the voltage applied to transistor 58 in the protection circuit 36 also slowly decays. However, Martin's voltage -V1 to the horizontal deflection yoke 17 is **not** slowly decayed, nor is the slowly decaying voltage of the protection circuit 36 in Martin provided to the deflection yoke 17. The slowly decaying voltage of the protection circuit 36 in Martin goes no further than the base of transistor 58, turning transistor 58 on long enough to draw extra current through deflection yoke 17 in order to drive the beam of the screen.

Therefore, the Board's statement on page 9, lines 13-17 is based on an erroneous

interpretation of Martin.

There remains only one other statement in the Board's decision indicating claim 1 would have been obvious. On page 11, line 14- page 12, line 20 the Board finds "an artisan would have been taught to provide the slow voltage decay circuit of the horizontal deflection control circuit 36 of Martin at the voltage source V1 of the [AAPA]," because:

- the AAPA recognizes that when power is interrupted, the high voltage charged on the horizontal deflection coil is not discharged; and
- Matin teaches when it is necessary to protect the screen, transistor 58 is turned on to draw additional current through the deflection coil so as to drive the beam off the screen.

As noted previously, although the AAPA recognizes that when power is interrupted, the high voltage charged on the horizontal deflection coil is not discharged, there is no teaching that this phenomena causes damage to the screen. Accordingly one of ordinary skill in the art would not have looked to Martin's screen protection system absent some teaching that the AAPA was subject to screen damage. Martin teaches that screen damage may occur if the beam is not driven off the screen when power is interrupted should protection circuit 34 fail.

If one of ordinary skill in the art is taught by Martin that the screen in the AAPA would be subject to damage, then one would have modified the AAPA to include Martin's protection circuit 36 including transistor 58 being connected to the AAPA's transistor TR in the same manner it is connected to Martin's transistor 56.

There has been no showing that provide the slow voltage decay circuit of the horizontal deflection control circuit 36 of Martin at the voltage source V1 of the AAPA would provide the

screen protection desired by Martin.

Accordingly, there is no *prima facie* showing that an artisan would have been taught to provide the slow voltage decay circuit of the horizontal deflection control circuit 36 of Martin at the voltage source V1 of the AAPA instead of at transistor TR in the same manner it is connected to Martin's transistor 56.

Again, it is only the Applicant's assessment of the phenomena of, when power is interrupted, the high voltage charged on the horizontal deflection coil is not discharged, which lead the Applicant to suggest that the horizontal output circuit 134 or the transistor TR in the horizontal output circuit 134 could possibly be damaged when power is returned. This in turn lead the Applicant to provide power interruption delay charging means for gradually lowering the input voltage to said horizontal/vertical processor constant voltage circuit.

Therefore, a display device derived from the combined teachings of the AAPA and Martin fails to teach a *power interruption delay charging means for gradually lowering said input voltage to said H/V processor constant voltage circuit when power supplied to said display device is interrupted.*

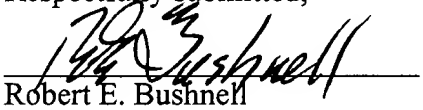
IX. CONCLUSION

It has been shown that the Board's decision:

- Includes a new ground of rejection;
- Fails to affirm the Examiner's rationale in support of the rejection;
- Erroneously holds that the AAPA, instead of the Applicant's assessment of the art, teaches that the horizontal output circuit 134 in the AAPA or transistor TR in horizontal output circuit 134 in the AAPA was subject to damage when power supplied to a display device is interrupted; and
- Fails to provide *prima facie* support for holding that the combined teaching would have suggested the invention set forth in claim 1.

Accordingly, the affirmation of the rejection of claims 1-11 is deemed to be in error and should be reversed.

Respectfully submitted,



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X. APPENDIX

CLAIMS UNDER APPEAL

1. A display device with a power interruption delay function, comprising:

a pulse width modulation controller for generating a pulse width modulation signal under the control of a microcomputer;

a current amplifier for amplifying current in response to the pulse width modulation signal from said pulse width modulation controller;

a H/V processor for generating a square wave pulse signal under the control of said microcomputer;

a horizontal driver for generating a drive pulse signal in response to the square wave pulse signal from said H/V processor;

a horizontal deflection coil for horizontally deflecting electron beams generated in said display device;

an S-correction capacitor connected in series between said horizontal deflection coil and a ground terminal, for correcting a linearity of center-to-left and right sides of a screen;

a horizontal output circuit for charging and discharging energy on said horizontal deflection coil and said S-correction capacitor in response to an output signal from said current amplifier and said drive pulse signal from said horizontal driver;

a H/V processor constant voltage circuit for supplying a constant voltage to said H/V processor in response to an input voltage; and

power interruption delay charging means for gradually lowering said input voltage to said H/V processor constant voltage circuit when power supplied to said display device is interrupted.

2. The display device as set forth in claim 1, wherein said power interruption delay charging means includes:

a polarity capacitor for performing a charging operation when power is supplied to said display device and a discharging operation when the power supplied to said display device is interrupted; and

a diode connected to said polarity capacitor, for preventing a voltage charged on said polarity capacitor from being discharged to a power supply circuit when the power supplied to the display device is interrupted.

3. A display device with a power interruption delay function, comprising:

a power supply circuit for converting a received commercial AC power into a DC input voltage;

a horizontal deflection circuit under the control of a microcomputer, receiving said DC input voltage, for horizontally deflecting electron beams generated in said display device; and

power interruption delay charging means for gradually lowering said DC input voltage received by said horizontal deflection circuit when said AC power supplied to said power supply circuit is interrupted, said power interruption delay charging means comprising:

a polarity capacitor for performing a charging operation when said AC power is supplied and a discharging operation when said AC power is interrupted; and

a diode connected to said polarity capacitor, for preventing a voltage charged on said polarity capacitor from being discharged to said power supply circuit when said AC power is interrupted.

4. The display device as set forth in claim 3, wherein said horizontal deflection circuit comprises:

a pulse width modulation controller for generating a pulse width modulation signal under the control of said microcomputer;

a current amplifier for amplifying current in response to said pulse width modulation signal generated by said pulse width modulation controller;

a H/V processor for generating a square wave pulse signal under the control of said microcomputer;

a horizontal driver for generating a drive pulse signal in response to the square wave pulse signal from said H/V processor;

a horizontal deflection coil for horizontally deflecting said electron beams;

a S-correction capacitor connected in series between said horizontal deflection coil and a ground terminal, for correcting a linearity of center-to-left and right sides of a screen;

a horizontal output circuit for charging and discharging energy on said horizontal deflection coil and said S-correction capacitor in response to an output signal from said current amplifier and said drive pulse signal from said horizontal driver; and

a H/V processor constant voltage circuit for supplying a constant voltage to said H/V processor in response to said DC input voltage, said DC input voltage being received through said power interruption delay charging means.

5. The display device as set forth in claim 4, wherein said current amplifier comprises:

a current amplification transformer having a primary coil and a secondary coil;

a field effect transistor FET1 having its gate terminal connected to one terminal of said secondary coil;

one terminal of said primary coil being connected to an output terminal of said pulse width modulation controller through a capacitor and another terminal of said primary coil being connected to said ground terminal;

said field effect transistor having a drain terminal connected to a high voltage source B+ and a source terminal connected in common to a second terminal of said secondary coil and one side of a pulse transformer;

said pulse transformer having a second side connected to one side of said horizontal deflection coil;

a first diode connected between said source terminal and said drain terminal; and

a second diode connected between said second terminal of said secondary coil and said ground terminal.

6. The display device as set forth in claim 5, wherein said horizontal output circuit comprises a horizontal output transistor having a collector terminal connected in common to said second side of said pulse transformer and said one side of said horizontal deflection coil, an emitter terminal connected to said S-correction capacitor and said ground terminal, and a base terminal connected to an output terminal of said horizontal driver for receiving said drive pulse signal.

7. The display device as set forth in claim 6, wherein said horizontal driver comprises:

a second field effect transistor having a gate terminal connected to receive said square wave pulse signal from said H/V processor, a source terminal connected to said ground terminal, and a

drain terminal;

a horizontal drive transformer having a primary coil and a secondary coil, said primary coil having one terminal connected to a voltage source through a resistor and a second terminal connected to said drain terminal of said second field effect transistor; and

said secondary coil of said horizontal drive transformer having one side connected to said base terminal of said horizontal output transistor and a second side connected to said ground terminal.

8. A display device with a power interruption delay function, comprising:

a pulse width modulation controller for generating a pulse width modulation signal under the control of a microcomputer;

a horizontal deflection coil for horizontally deflecting electron beams generated in said display device;

a current amplification transformer having a primary coil and a secondary coil;

a field effect transistor having its gate terminal connected to one terminal of said secondary coil;

one terminal of said primary coil being connected to an output terminal of said pulse width modulation controller through a capacitor and another terminal of said primary coil being connected to a ground terminal;

said field effect transistor having a drain terminal connected to a high voltage source and a source terminal connected in common to a second terminal of said secondary coil and one side of a pulse transformer;

said pulse transformer having a second side connected to one side of said horizontal

deflection coil;

a first diode connected between said source terminal and said drain terminal; and

a second diode connected between said second terminal of said secondary coil and said ground terminal;

a H/V processor for generating a square wave pulse signal under the control of said microcomputer;

a horizontal driver for generating a drive pulse signal in response to the square wave pulse signal from said H/V processor;

an S-correction capacitor connected in series between said horizontal deflection coil and a ground terminal, for correcting a linearity of center-to-left and right sides of a screen;

a horizontal output circuit for charging and discharging energy on said horizontal deflection coil and said S-correction capacitor in response to an output signal from said current amplifier and said drive pulse signal from said horizontal driver;

a H/V processor constant voltage circuit for supplying a constant voltage to said H/V processor in response to an input voltage; and

power interruption delay charging means for gradually lowering said input voltage to said H/V processor constant voltage circuit when power supplied to said display device is interrupted.

9. The display device as set forth in claim 8, wherein said power interruption delay charging means includes:

a polarity capacitor for performing a charging operation when power is supplied to said display device and a discharging operation when the power supplied to said display device is interrupted; and

a diode connected to said polarity capacitor, for preventing a voltage charged on said polarity capacitor from being discharged to a power supply circuit when the power supplied to the display device is interrupted.

10. The display device as set forth in claim 8, wherein said horizontal output circuit comprises a horizontal output transistor having a collector terminal connected in common to said second side of said pulse transformer and said one side of said horizontal deflection coil, an emitter terminal connected to said S-correction capacitor and said ground terminal, and a base terminal connected to an output terminal of said horizontal driver for receiving said drive pulse signal.

11. The display device as set forth in claim 10, wherein said horizontal driver comprises:

a second field effect transistor having a gate terminal connected to receive said square wave pulse signal from said H/V processor, a source terminal connected to said ground terminal, and a drain terminal;

a horizontal drive transformer having a primary coil and a secondary coil, said primary coil having one terminal connected to a voltage source through a resistor and a second terminal connected to said drain terminal of said second field effect transistor; and

said secondary coil of said horizontal drive transformer having one side connected to said base terminal of said horizontal output transistor and a second side connected to said ground terminal.